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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,181	12/02/2003	Richard Thomas Plunkett	PEA01US	6713
24011 7590 11/17/2008 SILVERBROOK RESEARCH PTY LTD 393 DARLING STREET BALMAIN, 2041 AUSTRALIA				
EXAMINER				
KAU, STEVEN Y				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/727,181

Applicant(s)

PLUNKETT ET AL.

Examiner

STEVEN KAU

Art Unit

2625

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 August 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☒ Claim(s) 5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date 9/15/2008
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Inventor's Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. Applicant's amendment was received on 8/12/2008, and has been entered and made of record. Currently, claims 1-5 are pending for further examination in this action.

Response to Remark/Arguments

2. Applicant's arguments with respect to claims 1-5 have been fully considered but are moot in view of the new ground(s) of rejection due to amendment.

Claim Objections

3. Claim 5 is objected to because of the following informalities: the limitation "according to claim 2, wherein, in repeated step (c)," does not have antecedence basis because claim 2 has been modified and step (c) is no longer in claim 2.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) (Shu' 839) and Young et al (US 6,154,195) (Young' 195) in view of Abe (US 5,471,325) (Abe' 325).

Regarding claim 1.

Shu' 839 discloses a method for sequentially outputting full lines of dither values of a dither matrix stored in a memory (**e.g. dither process for image reproduction and full lines of dither value are outputted from a memory, e.g. memory 738 of Fig. 5, col 10, lines 15-34**), comprising the step of:

(a) reading a plurality of dither values of the dither matrix from the memory, commencing at a start position in the memory until a full line of dither values of the dither matrix has been read (**e.g. identifying a line in the dither array for halftone process, it is a common sense that each dither line is selected for process and must start from the beginning of the line, col 10, lines 23-44**);

(b) updating the start position to an updated start position in the memory of a subsequent line of dither values (**e.g. since more than one dither lines are stored in the dither array, thus the next to the current line being processed must be updated to be a new line in order to continue for halftone processing, col 10, lines 35-48**); (d) repeating steps (a) - (c) until all lines of dither values of the dither matrix have been read and output to the buffer memory (**e.g. halftone processing is perform pixel by pixel; in addition, dither array is smaller than the image array and during dither process, dither array is repeated side by side over the image array to produce repetitive pattern, thus iteration of steps (a) to (c) must be performed, col**

8, lines 10-23).

Shu' 839 does not explicitly disclose (c) outputting the full line of dither values to a buffer memory; wherein after a first iteration of steps (a) - (c), steps (a) and (c) are performed simultaneously.

Young' 195 teaches (c) outputting the full line of dither values to a buffer memory **(e.g. dither value is stored back in the over sampling buffer 302 of Fig. 3, col 7, lines 47-50); and**

Abe' 325 teaches a concept of wherein after a first iteration of steps (a) - (c), steps (a) and (c) are performed simultaneously **(e.g. "two four-line buffers can be arranged in parallel and alternatively used for halftone discrimination and processing so that one line is dither-processing while another line is discriminated for the half-tone", col 10, lines 5-10).**

Having a method of sequentially outputting full lines of dither values of a dither matrix of Shu' 839 reference and then given the well-established teaching of Young' 195 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Shu' 839 reference to include outputting the full line of dither values to a buffer memory as taught by Young' 195 reference since doing so would increase the versatility of the method provided by Shu' 839 and further outputting dither values to a buffer memory provided by Young' 195 could easily be established for one another with predictable results; and then to modify the combination of Shu' 839 and Young' 195 to include the teaching of steps (a) and (c) are performed simultaneously since doing so would improve processing efficiency to

reducing processing time, and further, the concept of parallelism can be implemented with a predictable result.

Regarding claim 4, in accordance with claim 1.

Shu' 839 does not disclose wherein, in repeated step (c), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position.

Young' 195 teaches wherein, in repeated step (c), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position (**Young' 195 teaches outputting dither values to a buffer memory line by line in step (c), thus, the end of each line must be determined and a new line must be updated in order to have the halftone process performed properly, Fig. 3, col 7, lines 47-50).**

Having a method of sequentially outputting full lines of dither values of a dither matrix of Shu' 839 reference and then given the well-established teaching of Young' 195 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Shu' 839 reference to include in repeated step (c), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position as taught by Young' 195 reference since doing so would ensure the dither/half-tone performed properly and further outputting dither values to a buffer memory and updating line input provided by Young' 195 could easily be established for one another with predictable results.

Regarding claim 5, in accordance with claim 2.

Claim 5 recites identical features as claim 4. Thus, arguments similar to that presented above for claim 4 are also equally applicable to claim 5.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) (Shu' 839) and Young et al (US 6,154,195) (Young' 195) in view of Abe (US 5,471,325) (Abe' 325) as applied to claim 1 above, and further in view of Yamashita et al (Yamashita) (US 5,701,505).

Regarding claim 2, in accordance with claim 1.

Shu' 839 does not explicitly disclose wherein a plurality of dither matrices are stored in the memory, and wherein step (a) includes reading a plurality of dither values from at least two of the dither matrices simultaneously.

Yamashita' 505 discloses wherein a plurality of dither matrices are stored in the memory (**e.g. dither matrices are contained in the halftone circuits, which implies that dither matrices are stored in the memory of the circuitry, col 20, line 43 through col 21, line 11**), and wherein step (a), includes reading a plurality of dither values from at least two of the dither matrices simultaneously (**e.g. Yamashita discloses a parallel processing apparatus which processing data in block cycles, i.e. Fig. 27 teaches a process of outputting 4 lines; in order to support the parallel processing, the halftone-processing circuits 751-754 must reading at least two of the dither matrices simultaneously as shown in Figs 32-25 & col 20, line 63 through col 21, line 11**).

Having a method of sequentially outputting full lines of dither values of a dither matrix of Shu' 839 reference and then given the well-established teaching of Yamashita' 505 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Shu' 839, Young' 195 and Abe' 325 to include a plurality of dither matrices are stored in the memory, and wherein step (a) includes reading a plurality of dither values from at least two of the dither matrices simultaneously as taught by Yamashita' 505 reference since doing so would improve processing efficiency to reducing processing time, and further, the concept of parallelism can be implemented with a predictable result.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shu (US 5,594,839) (Shu' 839) and Young et al (US 6,154,195) (Young' 195) in view of Abe (US 5,471,325) (Abe' 325), and further in view of Yamashita et al (Yamashita) (US 5,701,505) as applied to claim 2 above, and further in view of Matsuba et al (Matsuba) (US 5,815,286).

Regarding claim 3, in accordance with claim 2.

Shu' 839 does not disclose wherein the dither matrices are of different sizes.

Matsuba' 286 discloses wherein the dither matrices are of different sizes (e.g. **four color components can be processed with respect to four threshold matrices value at the same time, Figs. 1a-c & col 7, lines 9-18 and col 20, lines 21-32).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the combination of Shu' 839, Young' 195, Abe'

325 and Yamashita' 505 to include that dither matrices are of different sizes taught by Matsuba' 286 and therefore, four color components can be processed with respect to four threshold matrices value at the same time (Figs 21A-D, col 20, lines 21-32).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Kau whose telephone number is 571-270-1120

and fax number is 571-270-2120. The examiner can normally be reached on Monday to Friday, from 8:30 am -5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Steven Kau/
Examiner, Art Unit 2625
11/12/2008

/David K Moore/
Supervisory Patent Examiner, Art Unit 2625